

REMARKS

Claims 1-38 are currently active.

The Examiner has rejected Claims 1-5, 16-20, 26, 33-35 as being anticipated by Holden. Applicant respectfully traverses this rejection. Applicant's claimed invention is a scheduler. The applied art of record is based on switching elements.

Referring to Holden, there is disclosed an apparatus for high-speed communications systems. Holden teaches an ATM network 10 having an input transmission line 110, input routing tables 120, an $N * N$ switch matrix 150, output routing tables 170, and output transmission lines 180. Associated with the input routing table 120 is a cell buffer memory 122 and configuration memory 124. Associated with the output routing table 170 is cell buffer memory 172 and configuration memory 174. See column 4, lines 26-36. Holden teaches ATM cells are sent through an input transmission line 110 into a connecting input routing table 120. The input routing table ascertains the cell's routing and determines an entry point into the cell switching matrix path. Cells are arranged in queues within a buffer memory 122 associated with the input routing table and then transmitted through the switch matrix 150. Upon exiting the switch matrix, cells are sent to one (or possibly more than one in the case of multicast cells) of the N output routing tables corresponding to the cells destination address. Within the output routing table 170, received cells are queued in a plurality of queues in cell

buffer 172 and subsequently transmitted onto a connecting output transmission line 180. See column 4, lines 37-54. In order to manage cells flowing through an ATM network, cells are grouped within the routing tables.

Holden teaches that switching elements are constructed to have 32 input ports and 32 output ports and are referred to as a quad switching element. Quad switching elements can be assembled into switch fabrics with a variety of configurations. One configuration of a switch fabric is made up of 20 Quad switching elements, arranged in four rows and five columns. A quad switching element may gang its output ports. Each quad switching element shown in figure 1 is configured into gangs of 16 output ports each and can route cells to one of 2 quad switching elements in a next stage. See column 5, lines 24-34.

Holden teaches that cells may be routed from one end of the switch fabric to the other end in a single cell time and are not queued anywhere in the switch fabric. See column 6, lines 14-16. The switching element inputs contain an elastic buffer on each input to allow cells traveling from different distances to be delayed in their arrival time into the switching element processing. This allows cells of all inputs to enter into the switching element routing processing at the same time to allow for effective routing an arbitration. See column 6, lines 35-40. Switching element outputs may be aggregated or ganged when multiple outputs are traveling into the same switching element in a next stage. See column 6, lines 42-45. Holden teaches a 32-input-quad switching element may be configured to operate as 216-port-switching

elements. This configuration allows one-half of the quad switching element to carry traffic in a forward direction and the other half to carry traffic in a reverse direction. See column 6, lines 57-61.

In the operation of a switching element, the switching element receives cells on input ports, determines a routing for cells to output ports, arbitrates which cells will actually be transmitted out of given output ports, and transmits those cells out of the output ports, and sends backpressure/knowledge signals in a reverse direction back to output ports. See column 6, line 65-column 7, line 5.

Holden teaches a specific switch element, called a WAC-488 contains the various features described above. The 488 implements a single element of a scalable switch fabric. The 488 has 32 input and 32 output ports, each containing a double-wide data interface, a start-of-cell signal, and a back pressure/acknowledge signal. The 488 can also be configured as a single 32 input * 32 output switch, or as 2 independent 16 input * 16 output switches. See column 10, lines 50-65.

Holden teaches a quad routing table can be used in a stand-alone application to support ATM switching. Four fabric interfaces are looped back to the quad routing table,. The quad routing table operates as an output buffer switch with no input cell buffering. See column 18, lines 45-51. Holden teaches the basic flow of cells for the quad routing table are

as follows. A cell enters the quad routing table on the receive side from the interface and the channel number is looked up. The cell is then either dropped or transferred to the receive cell buffer DRAM and queued in their receive queue controller depending upon 6 congestion management checks. When an available cell time occurs, 4 cells are selected by the receive side scheduler which reads the cells from the receive cell buffer DRAM and transmits them from the quad routing table into the switch fabric. Once a cell is received from the switch fabric of the transmit side, it is again either dropped or transferred to transmit cell buffer DRAM and queued in the transmit controller, depending upon 10 congestion management checks. When the cell is selected for transmission by the transmit side scheduler, it is removed from the transmit cell buffer DRAM and processed by the transmit multicast/header napper. The cell is then sent to the interface and exits the quad routing table on the transmit side. See column 21, lines 30-60.

As is eminently clear from the above description, the WAC that the examiner says is the first level generator, is a switching element and is not a scheduler, or a part of a scheduler. The quad routing table that the examiner says is the second level generator is also not a scheduler or any part of a scheduler but is a routing table. The Examiner must give deference to the specific terms that the applicant has used to define the claimed invention. The claims are all directed to a scheduler for a server, not a switching element, not a routing table, nor to emphasize a point a car, a bird or a diamond. In fact, in column 21, line 4, Holden teaches a receive side scheduler, and on column 21, line 52, Holden teaches a transmit side

scheduler. These are distinct elements from the WAC and from the quad routing table. It is these transmit side schedulers or receive side schedulers that applicant's scheduler could possibly be considered for use. However, Holden does not teach or suggest any details about the operation of the transmit side scheduler or the receive side scheduler.

Applicant's claimed invention is directed to the structure and operation of a scheduler. There's no teaching or suggestion in Holden of a switching element (the WAC) in combination with a quad routing table to somehow or other be configured to become a scheduler, and they cannot because they are each specific different types of elements of the switch. Accordingly, it is respectfully submitted that Holden has nothing at all to do with the design and architecture of a scheduler, but instead is teaching the operation of the overall switch having switching elements that comprise a switch fabric with input routing tables and output routing tables that are used to steer the connections through the switch fabric so they can be sent out toward the desired ultimate destination. The schedulers purpose which cells are to be serviced at any given time by the other components of the switch, as even taught by Holden and column 21, lines 41 and 52.

Accordingly, Claim 1 is not anticipated by Holden. Claims 2-5 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

Claim 16 is patentable for the reasons Claim 1 is patentable. Claims 17-20 are dependent to parent Claim 16 and are patentable for the reasons Claim 16 is patentable.

Claim 26 is patentable for the reasons Claim 1 is patentable. Claims 33-35 are patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claims 6-15, 21-25, 27-32 and 36-38 as being unpatentable over Holden in view of Lahat. Applicant respectfully traverses this rejection. Lahat does not add anything, in relevant part, to the teachings of Holden.

Referring to Lahat, there is disclosed an asynchronous transfer mode switch utilizing optical wave division multiplexing. Lahat teaches wave division multiplexing technology enables the simultaneous transmission of multiple data channel connections on the same physical optical fiber. This is achieved by utilizing several different wavelengths of the same optical fiber at the same time. See column 3, lines 37-41 of Lahat. Lahat teaches an ATM switch which utilizes an all optical switching fabric to form switching functions. The switch is based on fiber optics and dense wavelength division multiplexing. See column 4, lines 16-23.

The Examiner cites Lahat for the simple reason that Holden does not teach a bit map generator for generating schedule bitmap indicating the group to be scheduled for service.

Lahat does not teach or suggest a scheduler having a first level generator or a second level generator is found in Claim 1 or a scheduler that is based on a schedule bit map. For the reason that Holden nor Lahat teach or suggest the limitations of applicant's claimed invention, a scheduler, Holden in view of Lahat does not teach or suggest any of the claims of applicants.

In addition, Holden and Lahat cannot be combined. It is black letter patent law that there must be some teaching or suggestion in the references themselves to combine the references, and here there is none. Furthermore, the teachings of references cannot be taken out of the context in which they are found. Holden teaches a very specific type of a electrically based switch while Lahat teaches a completely distinct optically fiber based switch. The elements of each are not compatible with the other. They would not work. It is not a simple matter of identifying a given claim limitation in one reference and combining it with another claim limitation in another reference. It must be done so that it would be straightforward to do and not require significant redesign and development to somehow or other make applicant's claimed invention work. Here, to combine an optical switch with an electrical switch would required complete redesign and development. For this reason also, applicant's claims are not obvious from Holden and Lahat.

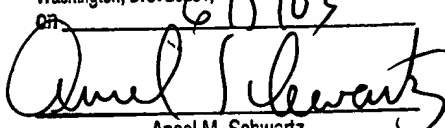
Moreover, it is clear the only reason that the Examiner is combining these references is through the use of hindsight from applicant's claimed invention. It is also not patent law to use hindsight from applicant's claims, nor to have applicant's claims serve as a

road map to find the various elements of applicant's claims and different limitations, and having found the various elements and different limitations, conclude that applicant's claimed invention is patentable. Accordingly, the applied art of record, separately or in combination, does not anticipate nor make obvious any of applicant's claims.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-38, now in this application be allowed.


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I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20531.

on 6/5/03

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